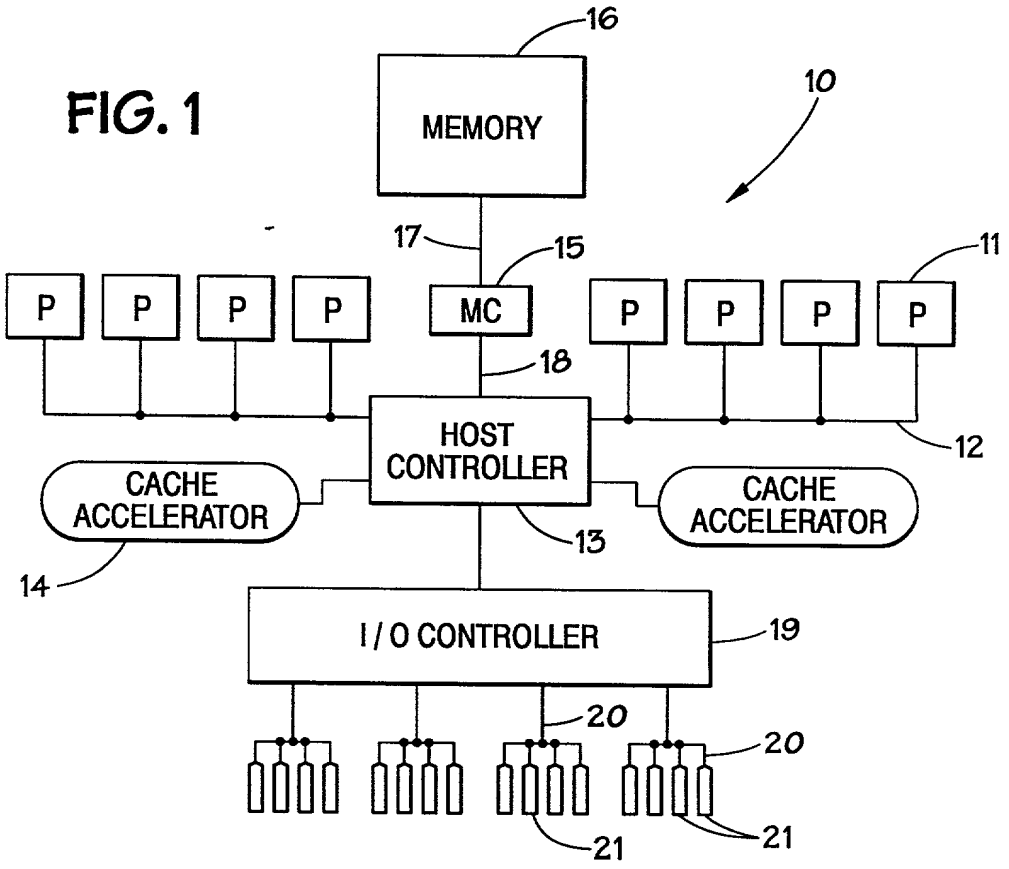
FIG. 1


16
MEMORY
10
17
15
11
P
P
P
P
MC
P
P
P
P
18
HOST CONTROLLER
12
CACHE ACCELERATOR
CACHE ACCELERATOR
13
14
I / O CONTROLLER
19
20
20
21
21

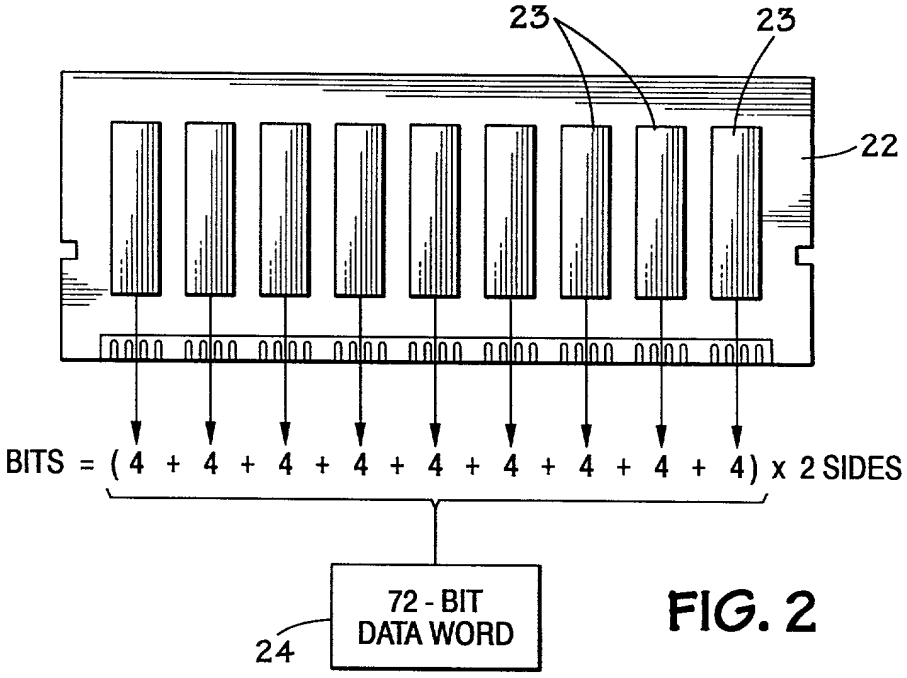

23
23
22
BITS = (4 + 4 + 4 + 4 + 4 + 4 + 4 + 4 + 4) x 2 SIDES
72 - BIT DATA WORD
24

FIG. 2

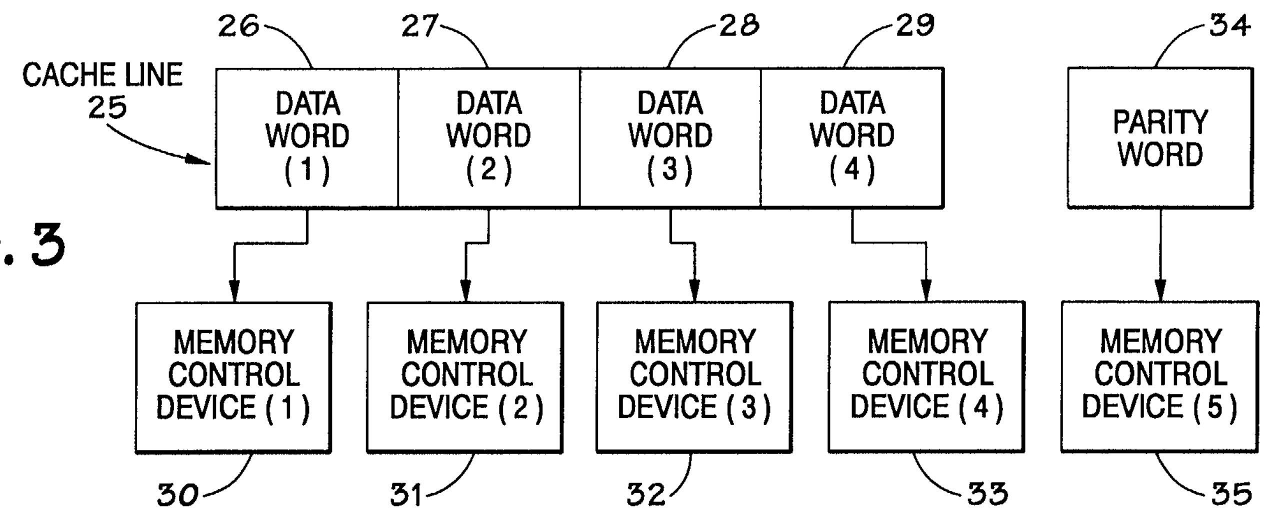

CACHE LINE
25
26
27
28
29
34
DATA WORD (1)
DATA WORD (2)
DATA WORD (3)
DATA WORD (4)
PARITY WORD
MEMORY CONTROL DEVICE (1)
MEMORY CONTROL DEVICE (2)
MEMORY CONTROL DEVICE (3)
MEMORY CONTROL DEVICE (4)
MEMORY CONTROL DEVICE (5)
30
31
32
33
35

FIG. 3

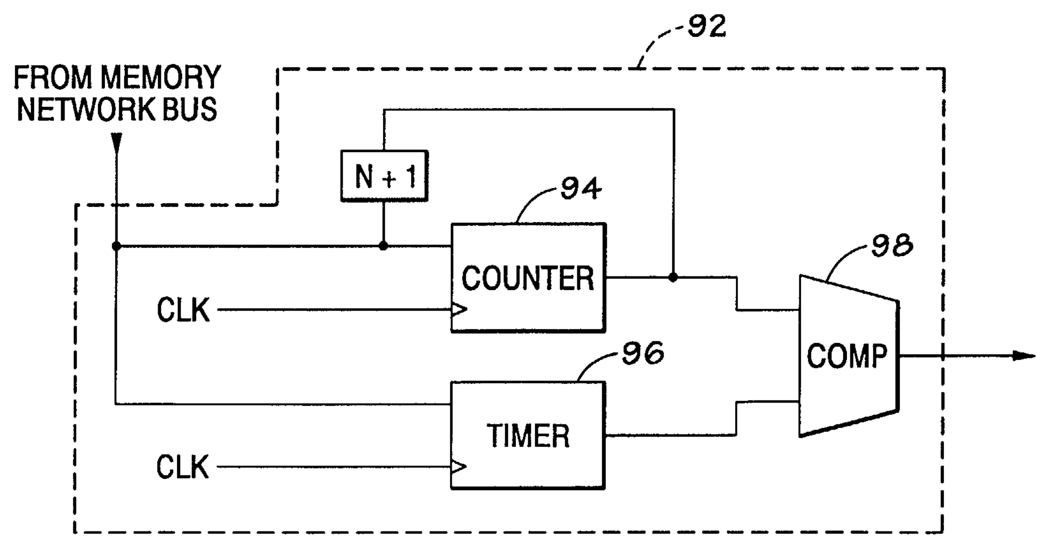

92
FROM MEMORY NETWORK BUS
N + 1
94
COUNTER
98
CLK
COMP
96
TIMER
CLK

FIG. 8

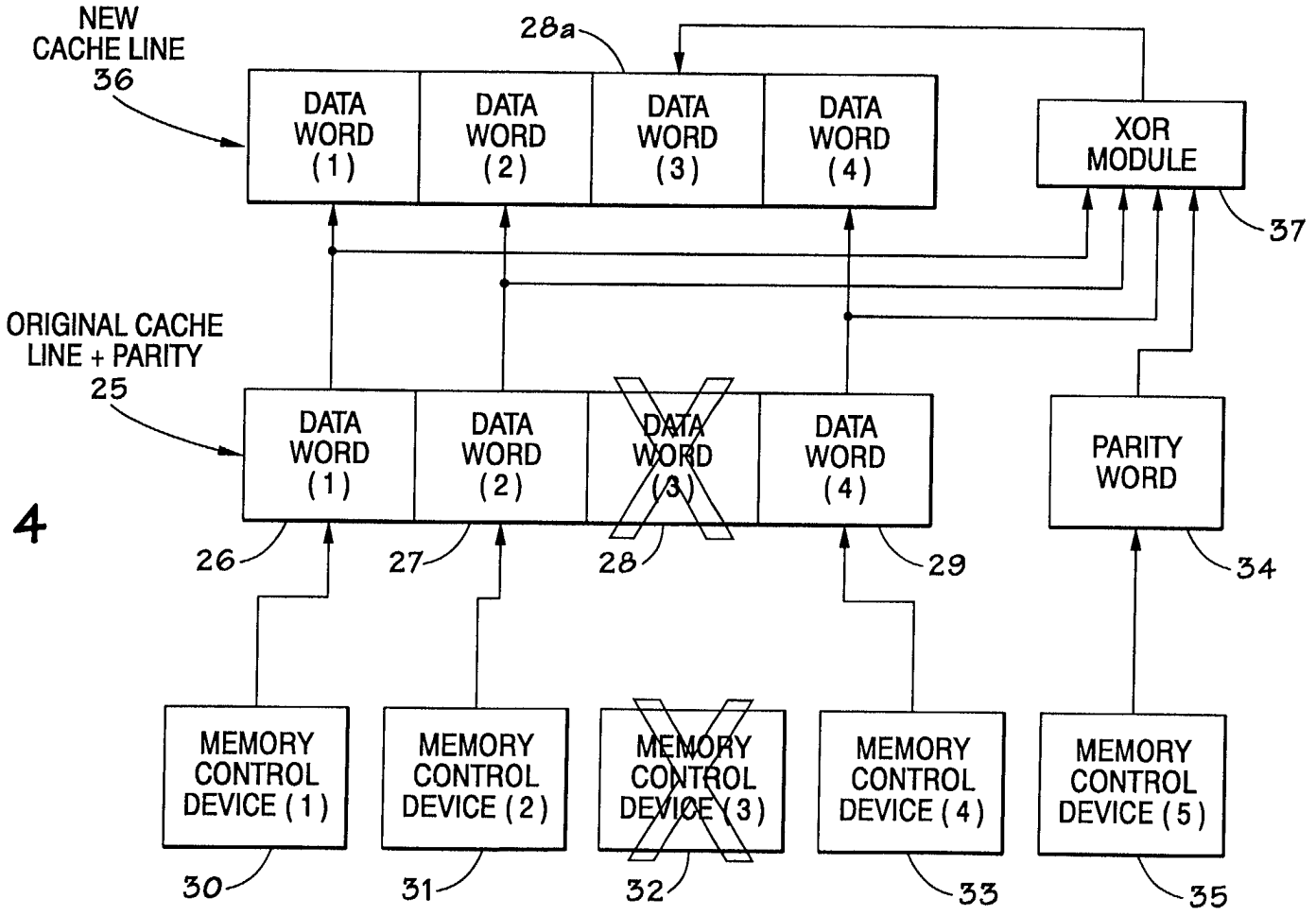


FIG. 4

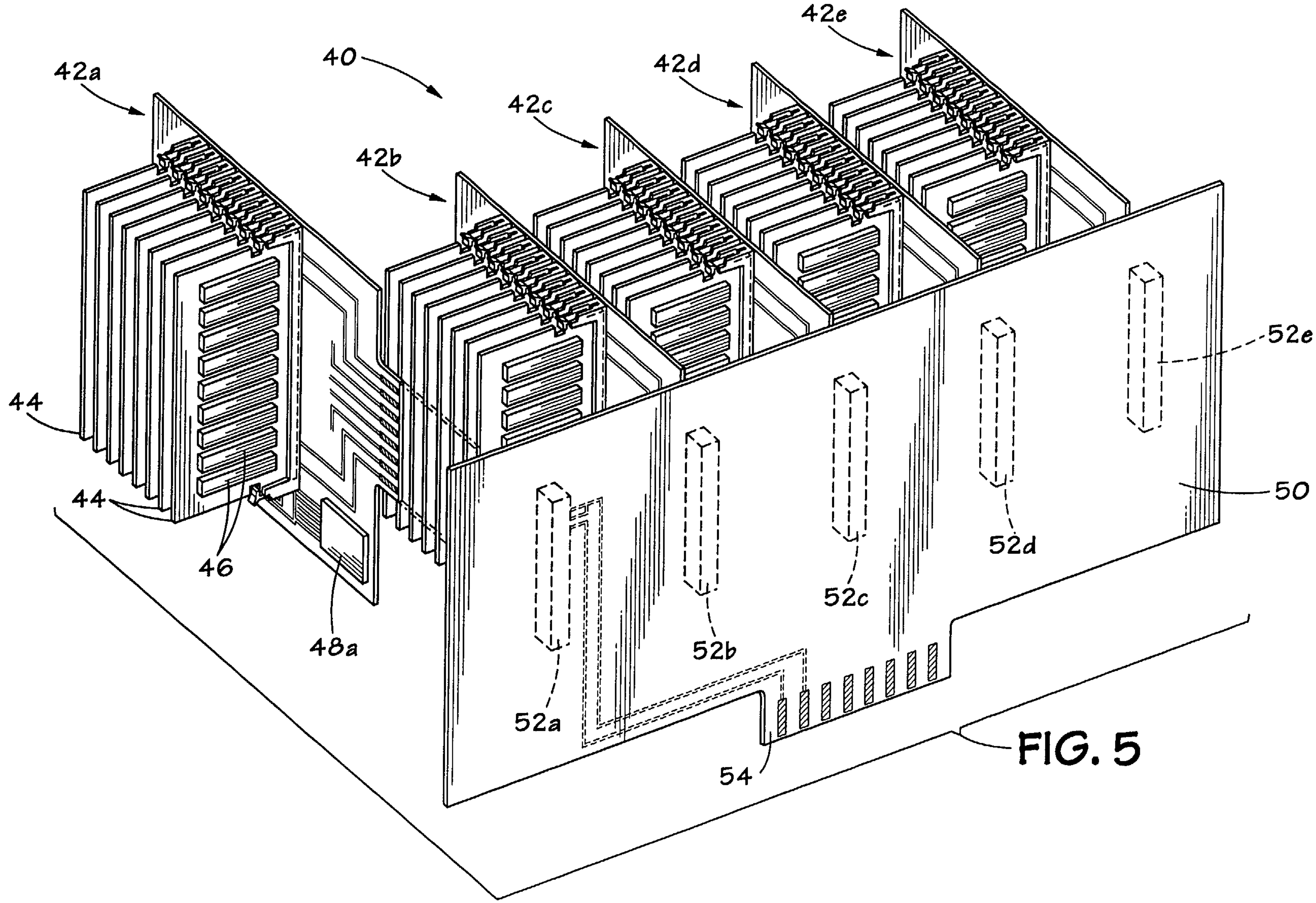


FIG. 5

FIG. 6

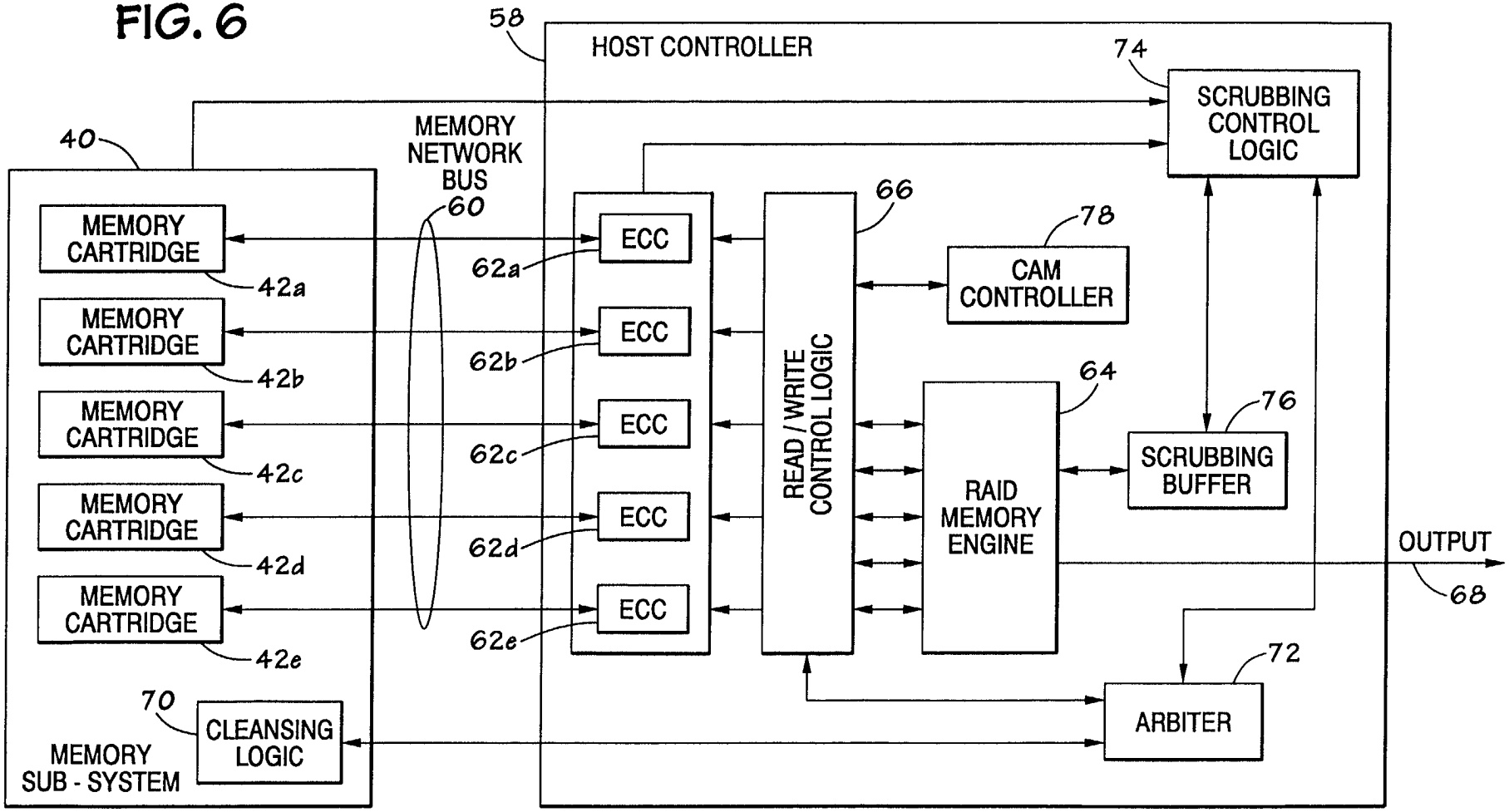
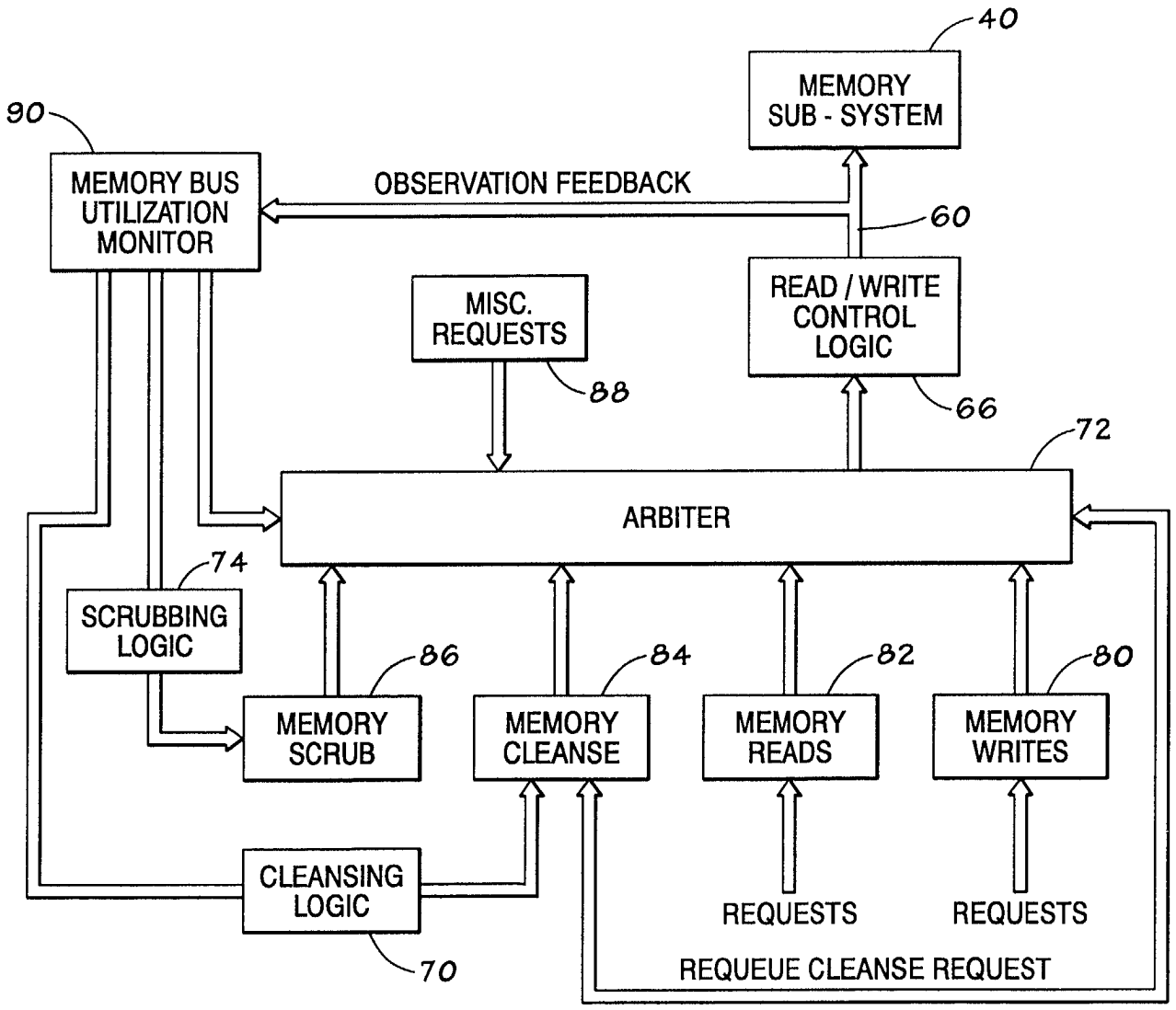


FIG. 7


40
MEMORY SUB - SYSTEM
90
MEMORY BUS UTILIZATION MONITOR
OBSERVATION FEEDBACK
60
READ / WRITE CONTROL LOGIC
MISC. REQUESTS
88
66
72
ARBITER
74
SCRUBBING LOGIC
86
84
82
80
MEMORY SCRUB
MEMORY CLEANSE
MEMORY READS
MEMORY WRITES
CLEANSING LOGIC
REQUESTS
REQUESTS
70
REQUEUE CLEANSE REQUEST